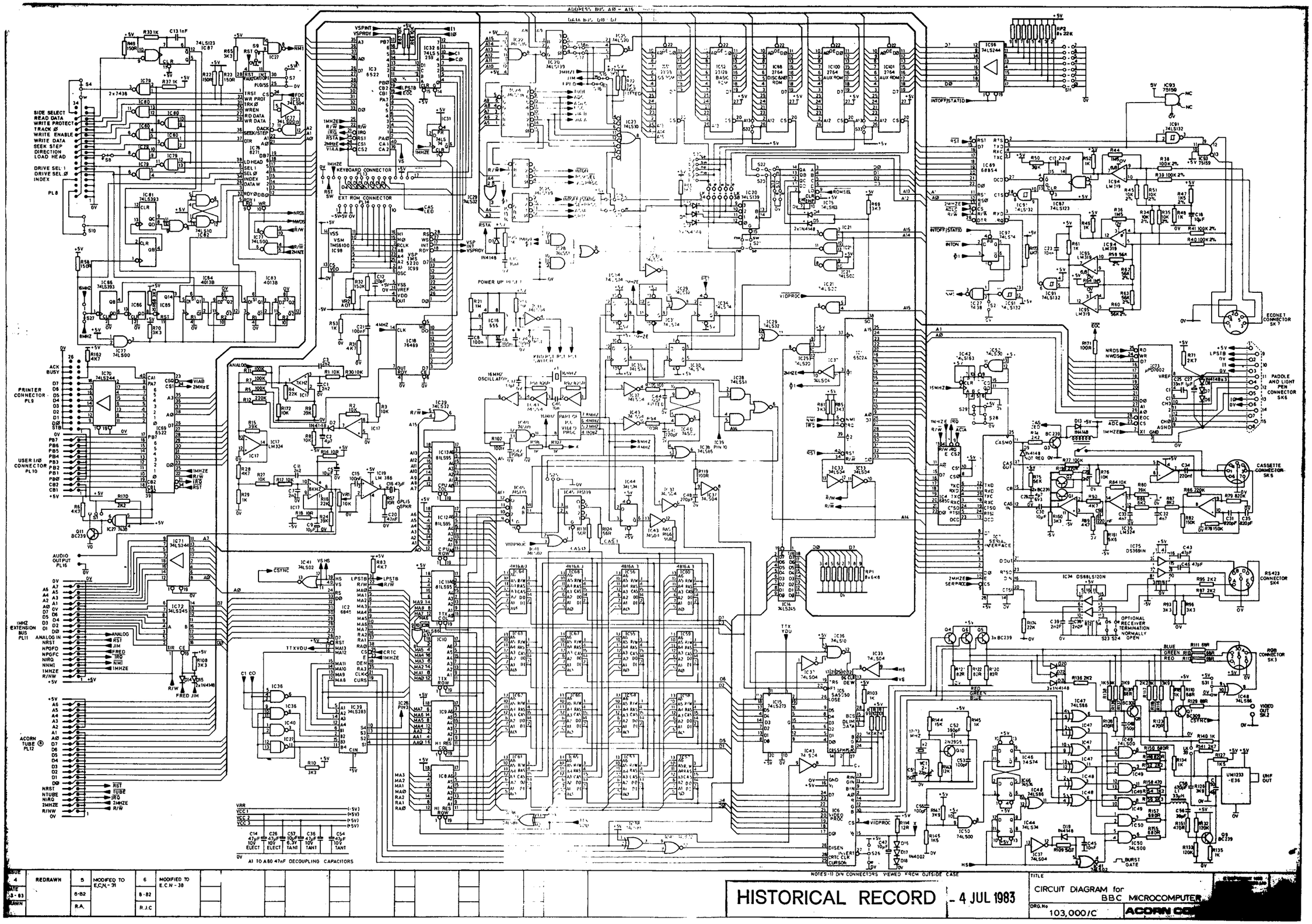
4	2	1	1	July 83


ADDRESS BUS A0 - A15
DATA BUS D0 - D7
SIDE SELECT
READ DATA
WRITE PROTECT
TRACK Ø
WRITE ENABLE
WRITE DATA
SEEK STEP
DIRECTION
LOAD HEAD
DRIVE SEL 1
DRIVE SEL Ø
INDEX
KEYBOARD CONNECTOR PL13
EXT ROM CONNECTOR PL14
POWER UP RESET
16MHZ OSCILLATOR
PRINTER CONNECTOR PL9
USER I/Ø CONNECTOR PL10
AUDIO OUTPUT PL16
1MHZ EXTENSION BUS PL11
ACORN TUBE Ⓡ PL12
ANALOG IN
VIDPROC
CRTC
ECONET CONNECTOR SK7
PADDLE AND LIGHT PEN CONNECTOR SK6
CASSETTE CONNECTOR SK5
RS423 CONNECTOR SK4
RGB CONNECTOR SK3
VIDEO OUT SK2
UHF OUT
A1 TO A80 47nF DECOUPLING CAPACITORS
NOTES-1) ON CONNECTORS VIEWED FROM OUTSIDE CASE
HISTORICAL RECORD - 4 JUL 1983
CIRCUIT DIAGRAM for BBC MICROCOMPUTER
DRG.No 103,000/C
ACORN CO
ISSUE 4 REDRAWN
DATE 3-83
DRAWN
5 MODIFIED TO E.C.N - 31 6-82 R.A.
6 MODIFIED TO E.C.N - 38 8-82 R.J.C

I.C. POWER PINS					
IC. REF	0V	+5V	IC. REF	0V	+5V
IC1	1,5	24	IC14	7	14
IC2	1,21	8	IC15	10	20
IC3	12	24	IC16	10	20
IC4	8	16	IC17	10	20
IC5	7	14	IC18	16	8
IC6	7	14	IC19	16	8
IC7	7	14	IC20	16	8
IC8	7	14	IC21	16	8
IC9	7	14	IC22	16	8
IC10	7	14	IC23	16	8
IC11	8	16	IC24	16	8
IC12	8	16	IC25	16	8
IC13	8	16	IC26	7	14
			IC27	7	14

ISSUE		B		C		D		1		2		3		4			
A	INITIAL ISSUE																
DATE	17-5-82	1-83		5.83		6-83		7.83	PPR 91	10-83	ECO 216	11-83	ECO 244	2-84	ECO 360		
DRAWN	RJC	RJC				CFD		MJ		BR		GCG		BR	3W		

TOLERANCE —
FINISH —
MATERIAL —

TITLE: 6502 2nd. PROCESSOR

DRG. No. A1/108,000/C

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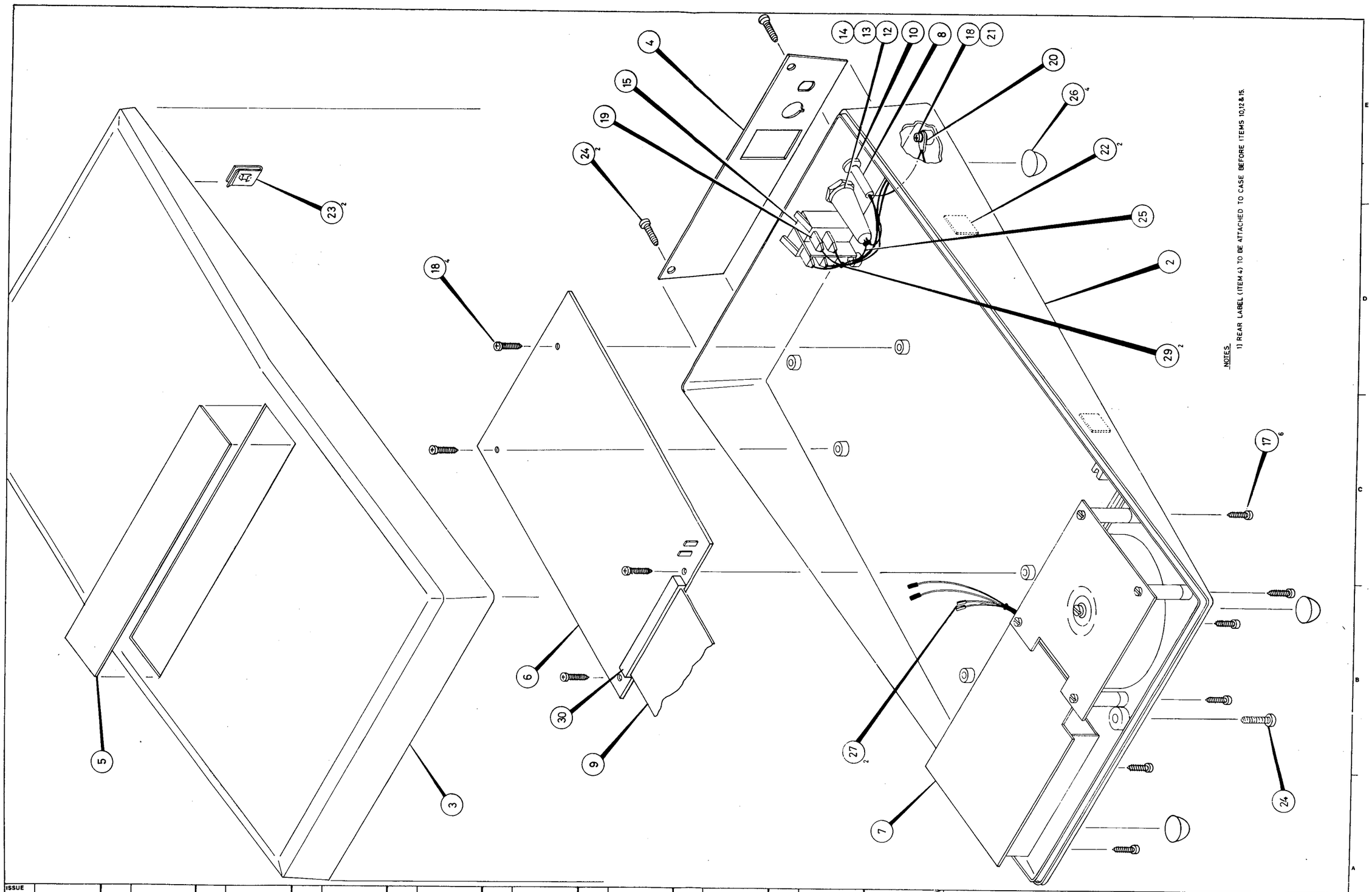
FULBOURN ROAD
CHERRY HINTON
CAMBRIDGE
CB1 4JN

ADMEL D/G/156

4	2	3	2	July 84



ISSUE 2	E.C.O 256	TOLERANCE	TITLE 6502 SECOND PROCESSOR MODULE GENERAL ASSEMBLY	©COPYRIGHT 1983 ACORN COMPUTERS Ltd FULBOURN ROAD CHERRY HINTON CAMBRIDGE CB1 4JN	
DATE 11-83		FINISH			
DRAWN J.S.C		MATERIAL SEE PARTS LIST	DRG. No. A1/008,000/A	ACORN COMPUTERS Ltd	

ADMEL D/G/156

IC No	0V	+5V	TYPE No.
1			TUBE
2			Z80
3	12	24	2372
4	10	20	81LS95
5	10	20	81LS95
6	16	8	8264
7	16	8	8264
8	16	8	8264
9	16	8	8264
10	16	8	8264
11	16	8	8264
12	16	8	8264
13	16	8	8264
14	8	16	74LS123
15	7	14	74S74
16	7	14	74LS74
17	7	14	74S74
18	7	14	74LS74
19	7	14	74LS132
20	7	14	74LS11
21	7	14	74LS00
22	7	14	74LS32
23	7	14	74LS32
24	7	14	74LS04
25	7	14	74LS04
26	7	14	74LS260
27	7	14	74LS133
28	10	20	81LS95
29	7	14	74LS32
30	7	14	74LS74

ISSUE																	
A	INITIAL ISSUE.	B	2732A ROM ADDED.	C	P.C.B RE-TAPED.	D	LK2 ADDED SRR SIGNAL DELETED.	E	LK3,LK4,R9 & D2 ADDED	1	PPR 90	2	ECO 197	3	ECO 403		
DATE	6.82			12.82		3.83		5.83		7.83		9.83		4.84			
DRAWN	R.A.			DBDL		M.J.		ACB		M.J.		J.L.T.		IRS			

TOLERANCE

FINISH

MATERIAL

TITLE: CIRCUIT DIAGRAM FOR Z80 2nd PROCESSOR

DRG. No. A1/0109,000/C

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ADMEL D/G/156